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Jiren YUAN	)	Group Art Unit: 2816
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For: Versatile Charge Sampling Circuits	)	

CLAIM FOR CONVENTION PRIORITY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The benefit of the filing date of the following prior foreign application in the following foreign country is hereby requested, and the right of priority provided in 35 U.S.C. § 119 is hereby claimed:

Swedish Patent Application No. 9903532-1

Filed: September 28, 1999

In support of this claim, enclosed is a certified copy of the prior foreign application. The prior foreign application was referred to in the oath or declaration. Acknowledgment of receipt of the certified copy is requested.

Respectfully submitted,

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VERSATILE CHARGE SAMPLING CIRCUITS

ABSTRACT

A charge sampling (CS) circuit samples a signal by integrating its current in a given time window, and the resulting charge represents the signal sample at the center time of the window. A band pass charge sampling (BPCS) circuit consists of two switches, a weighting-and-sampling (W&S) element, an integrator, and a control signal generator generating a clock, an inverse clock, a W&S signal and a resetting signal. Two ends of a differential signal are applied to the two switch inputs respectively. The two switches, controlled by the clock and the inverse clock respectively, are turned on alternately. Both switch outputs are fed to the W&S element input. The output of W&S element is fed to the integrator input. It works in three successive phases: resetting, sampling and holding. During the resetting phase, the integrator is reset by the resetting signal. Each sampling phase includes n clock cycles, during which the signal current is weighted in the W&S element and integrated in the integrator. During the holding phase, the integrator output is held. The CS and the BPCS circuits can have their differential and parallel versions. The sampling capacitors used in the CS and the BPCS circuits are much larger than that used in a voltage sampling circuit, resulting in low noise and low charge and clock feed-through. The BPCS circuit is simultaneously a filter, a mixer and a sampler, capable of working at radio frequencies. The center frequency, the bandwidth and the adjacent selectivity can be set by the clock frequency, the number n and the shape of W&S signal, particularly useful for front-end sampling radio receiver and system-on-chip.

BACKGROUND OF THE INVENTION

Voltage sampling is traditionally used for analog-to-digital (A/D) conversion. In a voltage sampler, a sampling switch is placed between a signal source and a capacitor. Between two sampling moments, the capacitor voltage tracks the signal voltage accurately. At the sampling moment, the switch is turned off to hold the capacitor voltage. The two processes become increasingly difficult when the signal frequency increases. For a given accuracy, thermal noise and switching noise set a minimum allowable capacitance while the tracking speed set a maximum allowable capacitance or switch resistance. It becomes impossible when the maximum is smaller than the minimum. Moreover, the clock jitter and finite turning-off speed (nonzero sampling aperture) make the sampling timing inaccurate. In fact, the bandwidth of a voltage sampling circuit must be much larger than the signal bandwidth. This makes direct sampling of high frequency radio signal extremely difficult. Sub-sampling can reduce the sampling rate but not the bandwidth of sampling circuit and not the demands on small clock jitter and small sampling aperture.

This invention uses charge sampling instead of voltage sampling. It does not track the signal voltage but to integrate the signal current. The bandwidth of charge sampling circuits does not have to be much larger than the signal bandwidth. The capacitor used to collect the charge can have very large capacitance to limit noises. Another important background is that for a radio signal, no matter how high is the carrier frequency, the signal bandwidth (the base band) remains a small fraction of the full band between DC to the carrier frequency. It is therefore unnecessary to convert the full band but just the band with the signal. The invented BPCS circuit fulfils this function exactly. In short, it is simultaneously a filter, a mixer and a sampler, particularly useful for front-end sampling radio receiver and system-on-chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a charge sampling (CS) circuit, and FIG. 1B and FIG. 1C are its working waveforms and frequency response respectively;
FIG. 2A is a band pass charge sampling (BPCS) circuit, and FIG. 2B is its working waveforms;
FIG. 3 is a differential BPCS circuit;
FIG. 4 is a parallel differential BPCS circuit;
FIG. 5 is an illustration of the filter function;
FIG. 6A and FIG. 6B are the ideal frequency response and output sample waveforms of a constant-weighting BPCS circuit with n=10 respectively;
FIG. 7A and FIG. 7B are the ideal frequency responses of a constant-weighting BPCS circuit with n=50 and n=500 respectively;
FIG. 8A and FIG. 8B are the ideal frequency responses of a linear-weighting BPCS circuit with n=50 and n=500 respectively;
FIG. 9A and FIG. 9B are the ideal frequency responses of a Gauss-weighting BPCS circuit with n=75, n=87, n=750 and n=870 respectively;
FIG. 10 is a differential BPCS circuit implementation;
FIG. 11A and FIG. 11B are the implementation with n=10 in constant weighting at 1000 MHz and the resulting frequency response respectively;
FIG. 12A and FIG. 12B are the implementation with n=59 in linear weighting at 1000 MHz and the resulting frequency response respectively;
FIG. 13A and FIG. 13B are the implementation with n=599 in linear weighting at 1000 MHz and the resulting frequency response respectively;
FIG. 14A and FIG. 14B are single ended and differential active integrators respectively;
FIG. 15 is a two-step BPCS circuit; and
FIG. 16 is a front-end sampling radio receiver architecture.

DETAILED DESCRIPTION OF THE DRAWINGS

1. In FIG. 1A, a charge sampling (CS) circuit 1 is shown. It consists of a sampling switch 2, an integrator 3 and a control signal generator 4 generating a sampling signal and a resetting signal. The shown type of the integrator 3 consists of a capacitor 3-1, a resetting switch 3-2 and an optional resistor 3-3. The integrator 3 may be in other types. An analog signal is applied to the input of the sampling switch 2. The charge sampling process involves three successive phases: resetting, sampling (t_1 to t_2) and holding. The time from t_1 to t_2 is defined as the sampling window. FIG. 1B shows its working waveforms. During the resetting phase, only the resetting switch 3-2 is turned on and the capacitor 3-1 is reset. During the sampling phase, only the sampling switch 2 is turned on, and the signal current is integrated onto the capacitor 3-1. The time constant is large enough to be able to obtain a linear charging when the signal comes from a voltage source (the usual case). If the on-resistance of the switch 2 is too small, the optional resistor 3-3 can be added. During the holding phase, both switches are in off-state, and the output voltage of the integrator 3 is held for further use. A pair of CS circuits can be used together to produce differential outputs to cancel common mode effects, using a differential input signal and sharing the control signal generator 4. The CS circuits or circuit pairs can be used in parallel to increase the sampling rate and to make the time interval between two sampling points possibly less than the sampling window, by time-interleaving both sampling and resetting signals. The signal current can be represented as $I(t)=\Sigma I_i\sin(\omega_i t+\phi_i)$, $i=1, 2, \ldots, m$. The total integrated charge is $Q=\Sigma Q_i$, where $Q_i=(I_i/\omega_i)(\cos(\omega_i t_1+\phi_i)-\cos(\omega_i t_2+\phi_i))$. If t_s is the center time of the sampling window, and $2\Delta t=(t_2-t_1)$ is the window width, $Q_i=(2\sin(\omega_i\Delta t)/\omega_i)I_i\sin(\omega_i t_s+\phi_i)=2\Delta t(\sin(\omega_i\Delta t)/(\omega_i\Delta t))I_i\sin(\omega_i t_s+\phi_i)$. Compared with the instant

value of the ith component at t_s, $I_i(t_s)=I_i\sin(\omega_i t_s+\phi_i)$, the difference is $k_i=2\Delta t(\sin(\omega_i\Delta t)/(\omega_i\Delta t))$, a sampling coefficient depending on frequency ω_i and Δt. With this coefficient, the ith frequency component has been precisely sampled at time t_s. Since all frequency components are sampled at t_s, the total charge on the capacitor naturally represents the signal sample at t_s, i.e. t_s is the equivalent sampling time point. The frequency response of the CS circuit depends on the function $\sin(\omega_i\Delta t)/(\omega_i\Delta t)$, shown in FIG. 1C. Its 3 dB bandwidth equals $\Delta f_{3dB}=1.4/(2\pi\Delta t)$, i.e. 1 GHz for a sampling window of 450 ps, independent of resolution. For voltage sampling, however, the sampling aperture must be smaller than 1 ps for an 8-bit resolution at 1 GHz. Since the function $\sin(\omega_i\Delta t)/(\omega_i\Delta t)$ is well defined, frequency compensation becomes possible. One way is to let the analog signal pass through a network with a frequency response of $(\omega_i\Delta t)/\sin(\omega_i\Delta t)$ before sampling. An alternative is to use digital signal processing (DSP) after A/D conversion to compensate the frequency response.

2. In FIG. 2A, a band-pass charge sampling (BPCS) circuit 5 is shown. It consists of two switches 2A and 2B, a weighting-and-sampling (W&S) element 6, an integrator 3 and a control signal generator 7 generating a clock, an inverse clock, a W&S signal and a resetting signal. Two ends of a differential analog signal are applied to the inputs of switches 2A and 2B respectively. The switches 2A and 2B, controlled by the clock and the inverse clock respectively, are turned on alternately. Both outputs of switch 2A and 2B are fed to the input of W&S element 6. The current passing through the W&S element 6 is controlled by the W&S signal. The output of W&S element 6 is fed to the input of integrator 3. Three successive phases are involved for each BPCS process: resetting, sampling and holding. FIG. 2B shows the working waveforms. During the resetting phase, the integrator is reset. Each sampling phase includes n clock cycles forming a sampling window. The signal current through W&S element equals zero outside the sampling window and is weighted according to the weighting function (constant, linear, Gauss or other fuctions) within the sampling window. The weighting function depends on the combination of the W&S element 6 and the W&S signal. The three W&S signals shown in FIG. 2B, corresponding to the three weighting functions (constant, linear and Gauss) are specifically used for a W&S element in which the current is linearly controlled by the W&S signal. During the holding phase, the output voltage of integrator 3 is held for further use.

3. In FIG. 3, a differential BPCS circuit 8 is shown. It consists of four switches 2A, 2B, 2C and 2D, a differential W&S (D-W&S) element 9, a differential integrator 10, and a control signal generator 7, as connected. The shown type of D-W&S element 9 consists of two parallel W&S elements 6A and 6B, and the shown type of differential integrator consists of two parallel integrators 3A and 3B. The D-W&S element 9 and the differential integrator 10 may be in other types. The differential BPCS circuit 8 works in the same way as the single ended BPCS circuit 5 except to produce two outputs differentially. The differential BPCS circuit 8 effectively cancels the common mode effects and gives more accurate results.

4. In FIG. 4, a parallel differential BPCS circuit 11 is shown. It consists of four switches 2A, 2B, 2C and 2D, a number of D-W&S elements 9A, 9B, ..., 9X, a number of differential integrators 10A, 10B, ..., 10X, a multiplexer (MUX) 12 and a control signal generator 13, as connected. Each pair of the D-W&S element and the differential integrator, 9A+10A, 9B+10B, ..., 9X+10X, together with the switches 2A, 2B, 2C and 2D work in the same way as the differential BPCS circuit 8. The W&S signals and the resetting signals to these pairs, generated by the control signal generator 13, are evenly time-interleaved. The MUX 12 multiplexes the outputs of the differential integrators 10A, 10B, ..., 10X to the differential outputs when they are in the holding phase, controlled by the multiplexing signals from the control signal generator 13. As a whole, the parallel BPCS circuit gives a higher sampling rate and makes the

time interval between two successive sampling points possibly less than the sampling window. If switches 2C and 2D are removed, and the differential W&S elements and the differential integrators are replaced by single-ended versions, it becomes a parallel single-ended BPCS circuit.

5. In FIG. 5, the filter function of the BPCS circuits is illustrated. From top-down, the frequency increases from DC to $3f_c$, where f_c is the clock frequency. Note that during the negative clock phase the same signal is connected oppositely, which is reflected in the diagram by changing the signal sign. The normalized amplitudes of resulting charges, i.e. the sums of the areas, integrated in n clock cycles are listed in FIG. 5 respectively. It is obvious that for input signals with frequencies much higher or lower than f_c, the charges cancel each other almost completely, resulting in nearly zero output. For input signals with certain frequencies like $f_c/4$, $f_c/2$, $2f_c$, ..., the charges are completely cancelled no matter what are their phases. For input signals with frequencies near to f_c, the charges are only partly cancelled. When $f_{in}=f_c$, the charges are fully added each other if it is in-phase with f_c while fully cancelled when it is in $\pi/2$ phase with f_c (not shown in FIG. 5). There is a bandwidth in which the signal charges can be effectively integrated. Outside the bandwidth, the signal charges are either completely or substantially cancelled. This is obviously a filter function. It means that the noise with frequencies outside the bandwidth will be cancelled as well.

6. In FIG. 6A, the ideal frequency response of a BPCS circuit is shown, corresponding to a mathematically accurate integration of the signal current in the sampling window. In FIG. 6A, n=10 and constant-weighting are assumed, meaning that the weight of the current is kept constant in the 10-clok-cycle sampling window. FIG. 6A shows the frequency response from $f_{in}=0$ to $f_{in}=8f_c$, where the y-axis is the maximum output amplitude of different frequency components normalized by the maximum output amplitude in the whole frequency range while the x-axis is input frequencies normalized by f_c. It can be seen that the same frequency response is repeated after $f_{in}>2f_c$ but with lower amplitudes. The output frequency f_{out} equals $|f_{in}-(2p-1)f_c|$ for $2(p-1)f_c \le f_{in} \le 2pf_c$, where p is an integer (≥ 1). When $f_{in}=(2p-1)f_c$, the output is a DC voltage, and its amplitude depends on the phase relation of f_{in} and f_c. For a given p, the same output frequency is obtained for input frequencies f_{in1} ($<(2p-1)f_c$) and f_{in2} ($>(2p-1)f_c$) when $(2p-1)f_c-f_{in1}=f_{in2}-(2p-1)f_c$, but their phases are different. FIG. 6B shows the output sample waveforms at different input frequencies with f_c=1000 MHz and both I (solid line) and Q (dots) phases. It shows that the BPCS circuit is a filter, a mixer and a sampler simultaneously.

7. In FIG. 7A and FIG. 7B, the ideal frequency responses of a constant-weighting BPCS circuit with n=50 and n=500 are shown respectively. FIG. 7A shows the frequency response with n=50 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.95f_c<f_{in}<1.05f_c$. FIG. 7B shows the frequency response with n=500 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.995f_c<f_{in}<1.005f_c$. It can be seen that $\Delta f_{3dB}=0.018f_c$ with n=50 and $\Delta f_{3dB}=0.0018f_c$ with n=500, i.e. the bandwidth is inversely proportional to n. The amplitudes of far-end frequency components are reduced with the increase of n, but the maximum adjacent peaks in both cases remain almost unchanged, around –13 dB.

8. In FIG. 8A and FIG. 8B, the ideal frequency responses of a linear-weighting BPCS circuit with n=50 and n=500 are shown respectively. Linear-weighting means that during the sampling phase the weight of the current is first linearly increase and then linearly decrease, symmetric to the center of the sampling window. FIG. 8A shows the frequency response with n=50 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.9f_c<f_{in}<1.1f_c$. FIG. 8B shows the frequency response with n=500 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.99f_c<f_{in}<1.01f_c$. It can

be seen that $\Delta f_{3dB}=0.025f_c$ with n=50 and $\Delta f_{3dB}=0.0025f_c$ with n=500, slightly increasing compared to the constant-weighting cases. The amplitudes of far-end frequency components are rapidly reduced with the increase of n. The maximum adjacent peaks are reduced to –26 dB and –27 dB respectively, compared to those of the constant-weighting cases.

9. In FIG. 9A and FIG. 9B, the ideal frequency responses of a Gauss-weighting BPCS circuit are shown. Gauss-weighting means that during the sampling phase the weight of the current varies according to the Gauss function $\exp(-t^2/2\sigma^2)$ for a given σ, symmetric to the center of the sampling window. The ratio $\Delta t/\sigma$, where Δt is half of the sampling window and σ the standard deviation, is a weighting parameter. FIG. 9A shows the frequency responses of n=75 with $\Delta t/\sigma=3.5$ and n=87 with $\Delta t/\sigma=4$ respectively in the range of $0<f_{in}<2f_c$. The 3 dB bandwidths are both $0.025f_c$. FIG. 9B shows the frequency responses of n=750 with $\Delta t/\sigma=3.5$ and n=870 with $\Delta t/\sigma=4$ respectively in the range of $0.9f_c<f_{in}<1.1f_c$. The 3 dB bandwidths are both $0.0025f_c$. The amplitudes of far-end frequency components and the adjacent peaks are substantially reduced with the Gauss-weighting. The maximum adjacent peaks are in the range of –61 dB to –78 dB.

10. In FIG. 10, an implementation 14 of the core of the differential BPCS circuit 8, using n-MOS transistors, is shown. The clocked switches are n-MOS transistors 15A, 15B, 15C and 15D. The W&S elements are n-MOS transistors 16A and 16B. The resetting switches are n-MOS transistors 18A and 18B. The capacitors are on-chip MOS capacitors 17A and 17B. The clocks are in sinuous waves but quasi-square waves can also be used. The implementation 14 works in all CMOS processes. Parameters of a 0.8 μm CMOS process, however, is used in the HSPICE simulations. The following three implementations are based on the implementation 14 with particular component values and W&S signal parameters.

11. In FIG. 11A, an implementation 19 with n=10 in constant-weighting at f_c=1000 MHz is shown. The clocked switches are n-MOS transistors 20A, 20B, 20C and 20D. The W&S elements are n-MOS transistors 21A and 21B. The resetting switches are n-MOS transistors 23A and 23B. They all have the minimum size, 2 μm/0.8 μm (width/length). The capacitors are MOS capacitors 22A and 22B, both 40 pF. The width of the constant-weighting W&S signal is 10 ns, corresponding to n=10. The maximum differential output sample voltage is around 100 mV. FIG. 11B shows both the theoretical frequency response in solid line and the HSPICE simulated frequency response in dots for f_{in}=900-1100 MHz. The simulated frequency response is closely in accordance with the theoretical frequency response. In both cases, the maximum adjacent peaks are –13 dB and Δf_{3dB}=18 MHz.

12. In FIG. 12A, an implementation 24 with n=59 in linear-weighting at f_c=1000 MHz is shown. The clocked switches are n-MOS transistors 25A, 25B, 25C and 25D, all having an increased size of 10 μm/0.8 μm. This makes the signal currents dominated by the W&S elements not the switches. The W&S elements are n-MOS transistors 21A and 21B, 2 μm/0.8 μm. The resetting switches are n-MOS transistors 23A and 23B, 2 μm/0.8 μm. The capacitors are MOS capacitors 22A and 22B, both 40 pF. The width of the linear-weighting W&S signal is 59 ns, corresponding to n=59. The maximum differential output sample voltage is around 100 mV. FIG. 12B shows the theoretical frequency response in solid line and the HSPICE simulated frequency response in dots for f_{in}=900-1100 MHz. The simulated frequency response is basically in accordance with the theoretical frequency response. Both have Δf_{3dB}=21 MHz. For the implementation 24, however, the maximum adjacent peak is –30 dB, lower than that of the theoretical response. This is because the conductance of n-MOS transistors 21A or 21B does not vary linearly with the linear W&S signal. The actual weighting function is somewhere between linear and Gauss.

13. In FIG. 13A, an implementation 26 with n=599 in linear weighting at f_c=1000 MHz is shown. The clocked switches are n-MOS transistors 25A, 25B, 25C and 25D, 10 μm/0.8 μm. The W&S elements are n-MOS transistors 27A and 27B, 2 μm/16 μm. Note that the lengths of 27A and 27B are increased to 16 μm to limit the signal current and the capacitor voltage during such a long charging period (599 ns). The resetting switches are n-MOS transistors 23A and 23B, 2 μm/0.8 μm. The capacitors are MOS capacitors 28A and 28B, both 20 pF. The width of the linear weighting W&S signal is 599 ns, corresponding to n=599. The maximum differential output sample voltage is around 100 mV. FIG. 13B shows the theoretical frequency response in solid line and the HSPICE simulated frequency response in dots for f_{in}=990-1010 MHz. The simulated frequency response is basically in accordance with the theoretical frequency response. Both have Δf_{3dB}=2 MHz. For the same reason mentioned above, the maximum adjacent peak of the implementation 26 is –30 dB, lower than that of the theoretical response.

14. In FIG. 14A and FIG. 14B, active integrators for improving output swing and linearity are shown respectively. A single ended active integrator 29 is shown in FIG. 14A. It consists of a differential-in-single-out amplifier 30, an inverter 35, a capacitor 31, and switches 32, 33 and 34, as connected. An active integrator always keeps the signal input at virtual ground, eliminating the impact of capacitor voltage on the signal current. The bandwidth of amplifier 30 needs only to cover the signal base-band not the carrier, which makes it feasible. The inverter 35 produces an inverted resetting signal with a delay, using the resetting signal as the input, to control the switch 33 while the resetting signal controls the switches 32 and 34. During the resetting phase, the switches 32 and 34 are turned on, and the switch 33 is turned off. The voltage of capacitor 31 is reset to the input offset voltage of the amplifier 30. During the sampling phase, the switches 32 and 34 are turned off and the switch 33 is turned on. The capacitor 31 is charged by the signal current. In the same time, the offset voltage of the amplifier 30 is cancelled. A differential active integrator 36 is shown in FIG. 14B. It consists of a differential-in-differential-out amplifier 37, two capacitors 31A and 31B, an inverter 35, and switches 32A, 32B, 33A, 33B, 34A and 34B. It works basically in the same way as the integrator 29 except uses a differential input signal and gives differential outputs. The integrator 29 can replace the integrator 3 while the integrator 36 can replace the integrator 10.

15. In FIG. 15, a two-step BPCS circuit 38 is shown. It consists of a first BPCS circuit 39, a chopping circuit 40, an amplifier 41, a second BPCS circuit 42, and a clock signal generator 43 generating a second clock. The first BPCS circuit 39 and the second BPCS circuit 42 can be any type of the BPCS circuits 5, 8, 11, 19, 24 and 26. To the first BPCS circuit 39, two ends of a differential analog signal are applied to its two inputs respectively, and a first clock is applied to its clock input. Signal samples with a first sample rate are produced from the first BPCS circuit 39 and fed to the chopping circuit 40. The samples are chopped symmetrically in time, controlled by the second clock. From the chopping circuit 40, the chopped signal with a new carrier frequency equal to the chopping frequency is fed to the amplifier 41, and the amplified differential signals are fed to two inputs of second BPCS circuit 42 respectively. Controlled by the second clock, the second BPCS circuit 42 produces the final sample output with a second sample rate. The two-step BPCS circuit 38 gives flexibility in performance trade-off. BPCS circuits in more steps can be built based on the two-step BPCS circuit 38.

16. In FIG. 16, a front-end sampling radio receiver architecture 44 is shown. It consists of a low pass filter 45 with $f_{pass}<2f_c$, a differential-out low noise amplifier (LNA) 46, two BPCS circuits 47A and 47B, a 90° phase shifter 48, and a local oscillator 49. The radio signal from antenna is applied to the input of the low pass filter 45. The frequency components above $2f_c$ are greatly attenuated. The output of the low pass filter 45 is fed to the LNA 46 to produce differential

outputs with a large enough amplitude. The differential outputs are fed to the inputs of BPCS circuits 47A and 47B simultaneously. In the same time, the I-clock signal produced by the local oscillator 49 is fed to the BPCS circuit 47A while the Q-clock signal reproduced by the 90° phase shifter 48 from the I-clock signal is fed to the BPCS circuit 47B. The BPCS circuits 47A and 47B produce I-samples and Q-samples respectively. The sample outputs can be either converted to digital data immediately or further treated. The BPCS circuits 47A and 47B can be any of the BPCS circuits 5, 8, 11, 19, 24 and 26. The integrators in these circuits can be either passive integrators or active integrators. The radio receiver architecture 44 has filtering, mixing and sampling functions simultaneously at the front-end, which relaxes the performance demands on A/D conversion, avoids analog filters, and highly utilizes the capability of DSP. In principle, any narrow bandwidth, i.e. any high Q value, is possible. The center frequency of the filtering function can be easily programmed. It is indeed a superior radio receiver architecture with a wide application scope.

ADVANTAGES

1. The frequencies of the signals possibly to be sampled by the CS circuits or the BPCS circuits are higher or much higher than that of the voltage sampling circuits at a given accuracy.

2. The sampling capacitors used in the CS circuits or the BPCS circuits are larger or much larger than the ones used in the voltage sampling circuits, giving advantages of low noise and low clock-and-charge feed-through.

3. Each BPCS circuit is simultaneously a filter, a mixer and a sampler, which greatly simplifies a radio receiver.

4. The BPCS circuits are capable of directly working at the radio frequency band, which makes a highly digitized radio receiver with front-end sampling and A/D conversion possible.

5. Both the center frequency and the bandwidth of a BPCS circuit can be easily programmed. The bandwidth can be as narrow as required, equivalent to have an unlimited Q-value.

6. The CS and BPCS circuits are simple and can be easily implemented in CMOS or other processes.

7. This technique is very useful for the purpose of system-on-chip, which requires a simple and highly digitized architecture.

CLAIMS

1. A charge sampling (CS) circuit and two of its differential versions; and
a CS circuit comprising:
a switch with a signal input, a signal output and a control input, to which an analog signal is applied to the signal input, and a sampling signal is applied to the control input, and in which the signal input is connected with the signal output only when said sampling signal is in the sampling phase, and the signal input is the signal input of said CS circuit; and
an integrator with a signal input, a signal output and a control input, to which the signal output of said switch is applied to the signal input, and a resetting signal is applied to the control input, and in which the current of said analog signal is integrated during said sampling phase, and the integrated charge produces a proportional voltage or current sample at the signal output at the end of said sampling phase, and said sample is held until the resetting phase of said resetting signal begins, and the time interval in between is the holding phase, and a series said samples are produced when said phases are repeated, and the signal output is the signal output of said CS circuit; and
a control signal generator with a clock input, a sampling signal output and a resetting signal output, to which a clock signal is applied to the clock input, and from which said resetting signal is generated at the resetting signal output, and said sampling signal is generated at the sampling signal output, and said resetting phase is followed by said sampling phase and then followed by said holding phase, and said phases are repeated, and in which the clock input is the clock input of said CS circuit; and
if said sampling phase is from time t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_s=(t_1+t_2)/2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin(2\pi f_i\Delta t))/(2\pi f_i \Delta t)$, where f_i is the frequency of the ith component of said analog signal and $\Delta t =(t_2-t_1)/2$, half of the width of said sampling phase; and
a first differential version of said CS circuit comprising:
a first CS circuit and a second CS circuit, to which two ends of a differential analog signal are applied to the signal input of said first CS circuit and the signal input of said second CS circuit respectively, and a clock signal is applied to the clock input of said first CS circuit, and in which the control signal generator of said first CS circuit is shared by said second CS circuit, and the control signal generator of said second CS circuit is omitted, and the signal input of said first CS circuit, the signal input of said second CS circuit, the clock input of said first CS circuit, the signal output of said first CS circuit and the signal output of said second CS circuit become the first signal input, the second signal input, the clock input, the first signal output and the second signal output of said first differential version of CS circuit; and
a second differential version of said CS circuit comprising:
a said first differential version of CS circuit with the inputs and outputs remaining the same names as the inputs and outputs of said second differential version of CS circuit respectively, in which the integrators in the first CS circuit and the second CS circuit of said first differential version of CS circuit are merged into a single differential integrator integrating the differential current of said analog signal and producing differential samples at the first signal output and the second signal output of said second differential version of CS circuit.

2. A band-pass charge sampling (BPCS) circuit and two of its differential versions; and
a BPCS circuit comprising:

Huvudfaxen Kassan

a first switch with a signal input, a signal output and a control input, to which the first end of a differential analog signal is applied to the signal input, and a clock is applied to the control input, and in which the signal input is connected with the signal output only when said clock is in on-state, and the signal input is the first signal input of said BPCS circuit; and

a second switch with a signal input, a signal output and a control input, to which the second end of said differential analog signal is applied to the signal input, and an inverse clock, the inversion of said clock to said first switch, is applied to the control input, and in which the signal input is connected with the signal output only when said second clock is in on-state, and the signal input is the second signal input of said BPCS circuit; and

a weighting-and-sampling (W&S) element with a signal input, a signal output and a control input, to which both the signal output of the first switch and the signal output of said second switch are applied to said signal input, and a W&S signal is applied to the control input, and in which the current of said analog signal passes through said W&S element only when said W&S signal is in the W&S phase containing n cycles of said clocks, and the current of said analog signal is controlled by said W&S signal in constant, linear, Gauss or other weighting functions; and

an integrator with a signal input, a signal output and a control input, to which the output of said W&S element is applied to the signal input, and a resetting signal is applied to the control input, and in which the current of said analog signal is integrated during said W&S phase, and the integrated charge produces a proportional voltage or current sample at the signal output at the end of said W&S phase, and said sample is held until the resetting phase of said resetting signal begins, and the time interval in between is the holding phase, and a series of samples are produced when said phases are repeated, and the signal output is the signal output of said BPCS circuit; and

a control signal generator with a clock input, a clock output, an inverse clock output, a W&S signal output and a resetting signal output, to which a clock signal is applied to the clock input, and from which said clock and said inverse clock are generated at the clock output and the inverse clock output respectively, and said resetting signal is generated at the resetting signal output, and said W&S signal is generated at the W&S signal output, and said resetting phase is followed by said W&S phase and then followed by said holding phase, and said phases are repeated, and the clock input is the clock input of said BPCS circuit ; and

said samples represent the base-band content of said analog signal, and the output frequency is $f_{out}= |f_{in}-(2p-1)f_c|$ for $2(p-1)f_c \le f_{in} \le 2pf_c$, where f_{in} is one of the frequency components of said analog signal, f_c the frequency of said clock and p an integer of ≥ 1 respectively, and the phase of said output frequency depends on the phase of said f_{in} and the phase of said f_c, and p=1 defines the major frequency response range, and the same shape of frequency response is repeated for p>1 but the amplitudes are reduced, and for a given p, the same output frequency is obtained for frequencies f_{in1} ($<(2p-1)f_c$) and f_{in2} ($>(2p-1)f_c$) when $(2p-1)f_c-f_{in1}=f_{in2}-(2p-1)f_c$ but with different phases, and the bandwidth and the shape of said frequency response depend on said n (the lager n, the narrower bandwidth) and said weighting function (constant, linear, Gauss or other functions), and said BPCS circuit is simultaneously a filter, a mixer and a sampler; and

a first differential version of said BPCS circuit comprising:

a first BPCS circuit and a second BPCS circuit, to which two ends of a differential analog signal are applied to the first signal input and the second signal input of said first BPCS circuit respectively, and in which the first signal input and the second signal input of said second BPCS circuit are connected with the second input and the first input of said first BPCS circuit respectively, and the control signal generator of said first BPCS circuit is

shared by said second BPCS circuit, and the control signal generator of said second BPCS circuit is omitted, and the first signal input, the second signal input, the clock input, and the signal output of said first BPCS circuit and the signal output of said second BPCS circuit become the first signal input, the second signal input, the clock input, the first signal output and the second signal output of said first differential version of BPCS circuit; and

a second differential version of said BPCS circuit comprising:

a said first differential version of BPCS circuit with the inputs and the outputs remaining the same names as the inputs and outputs of said second differential version of BPCS circuit, in which the integrators in said first BPCS circuit and said second BPCS circuit are merged into a single differential integrator integrating the differential current of said analog signal and producing differential samples at the first signal output and the second signal output of said second differential version of BPCS circuit.

3. A parallel CS circuit comprising:

a number of CS circuits according to claim 1, in which all first signal inputs are connected together as the first signal input of said parallel CS circuit, and all control signal generators in said CS circuits are omitted, and to which an analog signal is applied to the first signal input of said parallel CS circuit, and with which the parallel CS circuit is in a single ended version; or

a number of first or second differential version of CS circuits according to claim 1, in which all first inputs are connected together as the first signal input of said parallel CS circuit, and all second inputs are connected together as the second signal input of said parallel CS circuit, and all control signal generators of said CS circuits are omitted, and to which two ends of a differential analog signal are applied to the first signal input and the second signal input of said parallel CS circuit respectively, and with which the parallel CS circuit is in a differential version; and

a control signal generator with a clock input, said number of sampling signal outputs, said number of resetting signal outputs and said number of multiplexing signal outputs, to which a clock signal is applied to the clock input, and the clock input is the clock input of said parallel CS circuit, and from which said number of sampling signals are generated at the sampling signal outputs and fed to the control inputs of the switches of said CS circuits respectively, and said number of resetting signals are generated at said resetting signal outputs and fed to the control inputs of the integrators of the CS circuits respectively, and said number of multiplexing signals are generated at the multiplexing signal outputs, and said resetting signals, said sampling signals and said multiplexing signals are evenly time-interleaved; and

a multiplexer with said number signal inputs or input pairs (in the differential case, the same below), said number of control inputs, and a signal output or output pair, to which the signal outputs or output pairs of said CS circuits are applied to the signal inputs or input pairs respectively, and said multiplexing signals are applied to the control inputs respectively, and through which the outputs or output pairs of said CS circuits are multiplexed to the output or output pair of said parallel CS circuit when the outputs or output pairs of said CS circuits are in holding phases; and

said parallel CS circuit increases the sampling rate and makes the time interval between two successive sampling points possibly less than the sampling window according to claim 1.

4. A parallel BPCS circuit according to claim 2 comprising:

a number of BPCS circuits according to claim 2, in which all first signal inputs are connected together as the first signal input of said parallel BPCS circuit, all second signal inputs are connected together as the second signal input of said parallel BPCS circuit, and all the first

switches can be merged, and all the second switches can be merged, and all control signal generators in said BPCS circuits are omitted, and to which two ends of a differential analog signal is applied to the first signal input and the second signal input of said parallel BPCS circuit, and with which the parallel BPCS circuit is in a single ended version; or

a number of first or second differential version of BPCS circuits according to claim 2, in which all first signal inputs are connected together as the first signal input of said parallel BPCS circuit, and all second signal inputs are connected together as the second signal input of said parallel BPCS circuit, and all the first switches in said first BPCS circuits can be merged, and all the second switches in said first BPCS circuits can be merged, and all the first switches in said second BPCS circuits can be merged, and all the second switches in said second BPCS circuits can be merged, and all control signal generators of said BPCS circuits are omitted, and to which two ends of a differential analog signal are applied to the first signal input and the second signal input of said parallel BPCS circuit, and with which the parallel BPCS circuit is in a differential version; and

a control signal generator with a clock input, a clock output, an inverse clock output, said number of W&S signal outputs, said number of resetting signal outputs and said number of multiplexing signal outputs, to which a clock signal is applied to the clock input, and the clock input is the clock input of said parallel BPCS circuit, and from which a clock is generated at the clock output and fed to the control inputs of all first switches of said BPCS circuits, and an inverse clock is generated at the inverse clock output and fed to the control inputs of all second switches of said BPCS circuits, and said number of W&S signals are generated at the W&S signal outputs and fed to the control inputs of all W&S elements of said BPCS circuits, and said number of resetting signals are generated at the resetting signal outputs and fed to the control inputs of all integrators of said BPCS circuits, and said number of multiplexing signals are generated at the multiplexing signal outputs, and said resetting signals, said sampling signals and said multiplexing signals are evenly time-interleaved; and

a multiplexer with said number of signal inputs or input pairs, said number of control inputs, and a signal output or output pair, to which the signal outputs or output pairs of said BPCS circuits are applied to the signal inputs or input pairs respectively, and said multiplexing signals are applied to the control inputs respectively, and through which the outputs or output pairs of said BPCS circuits are multiplexed to the signal output or output pair when the signal outputs or output pairs of said BPCS circuits are in holding phases, and the signal output or output pair is the signal output or output pair of said parallel BPCS circuit; and

said parallel BPCS circuit increases the sampling rate and makes the time interval between two successive sampling points possibly smaller than the width of said W&S signal according to claim 2.

5. A frequency compensated CS circuit according to claims 1 and 3 comprising:

a CS circuit, or a first differential version of CS circuit, or a second differential version of CS circuit, according to claim 1; or

a signal ended version or a differential version of parallel CS circuit according to claim 3; and

an analog frequency compensating circuit with a signal input or input pair, and a signal output or output pair, with a frequency response proportional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$ according to claim 1, to which an analog signal is applied to the signal input or input pair, and from which the signal output is applied to the signal input of said CS circuit or the single ended version of said parallel CS circuit, or the signal output pair is applied to the first signal input and the second signal input of said first or second differential version of CS circuit or the differential version of said parallel CS circuit; or

a digital frequency compensating circuit with a frequency response proportional to $(2\pi f_i\Delta t)/(\sin(2\pi f_i\Delta t))$ according to claim 1 is connected after an A/D converter converting the signal output or output pair of said CS circuits or parallel CS circuits to a digital signal.

6. A two-step BPCS circuit according to claims 2 and 4 comprising:
   a first BPCS circuit in any type according to claims 2 and 4, to which two ends of a differential analog signal is applied to the first signal input and the second signal input respectively, and a clock signal is applied to the clock input as the first clock, and said first signal input, the second signal input and the clock input are the first signal input, the second signal input and the clock input of said two-step BPCS circuit, and from which signal samples are produced at the signal output or output pair with a first sample rate; and
   a chopping circuit with a signal input or input pair, a signal output or output pair, and a clock input, to which the signal output or output pair of said first BPCS circuit is applied to the signal input or input pair, and a second clock with a frequency equal to said first sample rate is applied to the clock input, and in which the signal is chopped symmetrically in time at the signal output or output pair with the frequency of said second clock; and
   a differential-out amplifier with a signal input or input pair and a signal output pair, to which the signal output or output pair of said chopping circuit is applied to the signal input or input pair, and in which the signal is amplified differentially at the signal output pair; and
   a second BPCS circuit in any type according to claims 2 and 4, to which the signal output pair of said amplifier is applied to the first signal input and the second signal input respectively, and said second clock is applied to the clock input, and from which signal samples are produced at the signal output or output pair with a second sample rate; and
   a clock signal generator with a clock input and a clock output, to which said first clock signal is applied to said clock input, and from which a second is generated at the clock output and simultaneously fed to the clock input of said chopping circuit and the clock input of said second BPCS circuit; and
   arrangements with more steps can be constructed based on said two-step BPCS circuit.

7. Arrangements of building blocks in any type of said CS and BPCS circuits according to claims 1, 2, 3, 4, 5 and 6; and
   an n-MOS arrangement of said switch comprising:
      an n-MOS transistor with the drain as the signal input, with the gate as the control input and with the source as the signal output; and
   a CMOS arrangement of said switch comprising:
      an n-MOS transistor and a p-MOS transistor with their drains connected each other as the signal input, with their sources connected each other as the signal output, and with the gate of said n-MOS transistor as the control input; and
      an inverter with the input connected to the gate of said n-MOS transistor and with the output connected to the gate of said p-MOS transistor; and
   an arrangement of said W&S element comprising:
      an n-MOS transistor with the drain as the signal input, with the gate as the control input, and with the source as the signal outpu; and
   an passive arrangement of said integrator comprising:
      a capacitor with the first end as the signal input, and with the second end grounded; and
      an optional resistor inserted between said signal input and the first end of said capacitor when necessary; and
      an n-MOS transistor with the drain and the source connected to the first end and second end of said capacitor respectively, and with the gate as the control input; and
   an passive arrangement of said differential integrator comprising:

Huvudfaxen Kassan

a first passive arrangement of said integrator with the signal input and the signal output as the first signal input and the first signal output of said differential integrator respectively; and

a second passive arrangement of said integrator with the signal input and the signal output as the second signal input and the second signal output of said differential integrator respectively; and

an active arrangement of said integrator comprising:

a differential-in-single-out amplifier with the positive input grounded, with the negative input as the signal input of said integrator, and with the output as the signal output of said integrator; and

a capacitor with the first end connected to the negative input of said differential-in-single-out amplifier; and

an inverter with the input as the control input of said integrator; and

a first n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the negative input of said differential-in-single-out amplifier, with the control input connected to the control input of said integrator, and with the signal output connected to the output of said differential-in-single-out amplifier; and

a second n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said capacitor, with the control input connected to the control input of said integrator, and with the signal output grounded; and

a third n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said capacitor, with the control input connected to the output of said inverter and with the signal output connected to the output of said differential-in-single-out amplifier; and

an optional resistor inserted between the signal input of said integrator and the negative input of said differential-in-single-out amplifier when necessary; and

an active arrangement of said differential integrator comprising:

a differential-in-differential-out amplifier with the negative input, the positive input, the positive output and the negative output as the first signal input, the second signal input, the first signal output and the second signal output of said differential integrator; and

a first capacitor with the first end connected to the negative input of said differential-in-differential-out amplifier; and

a second capacitor with the first end connected to the positive input of said differential-in-differential-out amplifier; and

an inverter with the input as the control input of said differential integrator; and

a first n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the negative input of said differential-in-differential-out amplifier, with the control input connected to the control input of said differential integrator and with the signal output connected to the positive output of said differential-in-differential-out amplifier; and

a second n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said first capacitor, with the control input connected to the control input of said differential integrator and with the signal output grounded; and

a third n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said first capacitor, with the control input connected to the output of said inverter and with the signal output connected to the positive output of said differential-in-differential-out amplifier; and

a fourth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the positive input of said differential-in-differential-out amplifier, with the control input connected to the control input of said differential integrator and with the

signal output connected to the negative output of said differential-in-differential-out amplifier; and

a fifth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said second capacitor, with the control input connected to the control input of said differential integrator and with the signal output grounded; and

a sixth n-MOS arrangement or CMOS arrangement of said switch with the signal input connected to the second end of said second capacitor, with the control input connected to the output of said inverter and with the signal output connected to the negative output of said differential-in-differential-out amplifier; and

a first optional resistor inserted between the first signal input of said differential integrator and the negative input of said differential-in-differential-out amplifier when necessary; and

a second optional resistor inserted between the second signal input of said differential integrator and the positive input of said differential-in-differential-out amplifier when necessary.

8. A front-end sampling radio receiver architecture using said BPCS circuits according to claims 2, 4, 6 and 7, comprising:

a low pass filter with a signal input or input pair and a signal output or output pair and with a bandwidth up to twice the clock frequency, to which a radio signal is applied to the signal input or input pair; and

a low noise amplifier with a signal input or input pair and a signal output pair, to which the output or output pair of said low pass filter is applied to the signal input or input pair, and from which a differentially amplified radio signal is produced at the signal output pair; and

a local oscillator with a signal output, from which an I-clock signal is produced at the signal output; and

a $\pi/2$ phase shifter with a signal input and a signal output, to which said I-clock signal is applied to the signal input, and from which a Q-clock signal is produced at the signal output with the same amplitude and $\pi/2$ phase shift with respect to said I-clock signal; and

a first BPCS circuit and a second BPCS circuit in any type according to claims 2, 4, 6 and 7, to which two ends of the signal output pair of said low noise amplifier are respectively applied to the first signal inputs and the second signal inputs of both said first BPCS circuit and said second BPCS circuit respectively, and said I-clock signal is applied to the clock input of said first BPCS circuit, and said Q-clock signal is applied to the clock input of said second BPCS circuit, and from which the base-band I-samples of said radio signal are produced at the signal output or output pair of said first BPCS circuit, and the base-band Q-samples of said radio signal are produced at the signal output or output pair of said second BPCS circuit; and

said local oscillator, said phase shifter and the clock generators of said first and second BPCS circuits can be combined to produce differential I-clock signals and Q-clock signals more efficiently and accurately; and

said base-band I-sample and Q-samples can be further converted either by two separate analog-to-digital converters or by a single analog-to-digital converter with multiplexing to digital signals; and

said digital signals can be further processed by a digital signal processing (DSP) unit; and

said front-end sampling radio receiver architecture is a superior radio receiver architecture, in which analog part is greatly simplified and the capability of DSP is highly utilized.

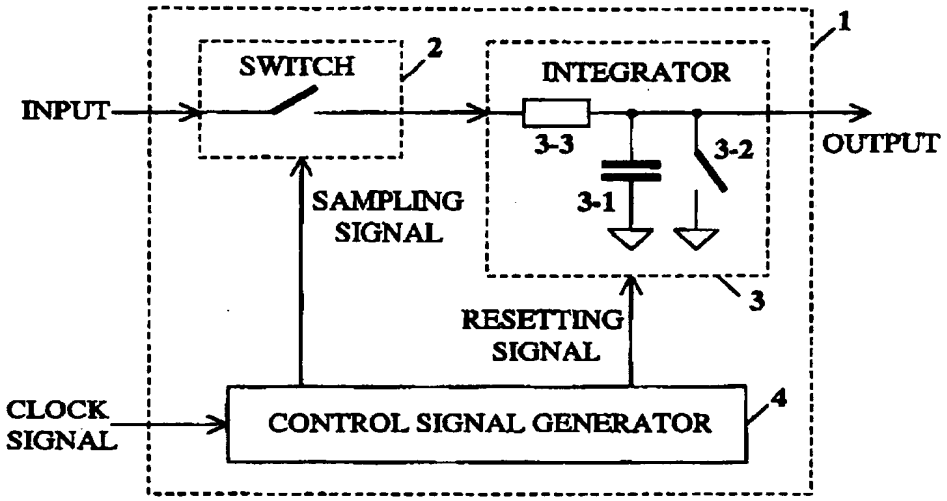


FIG. 1A

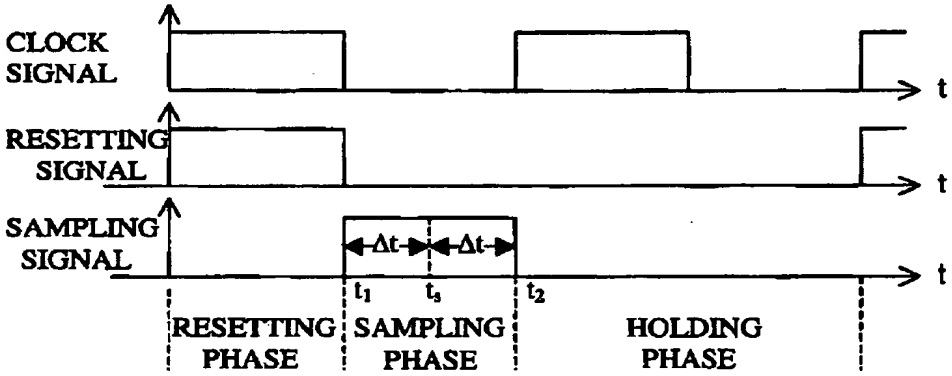


FIG. 1B

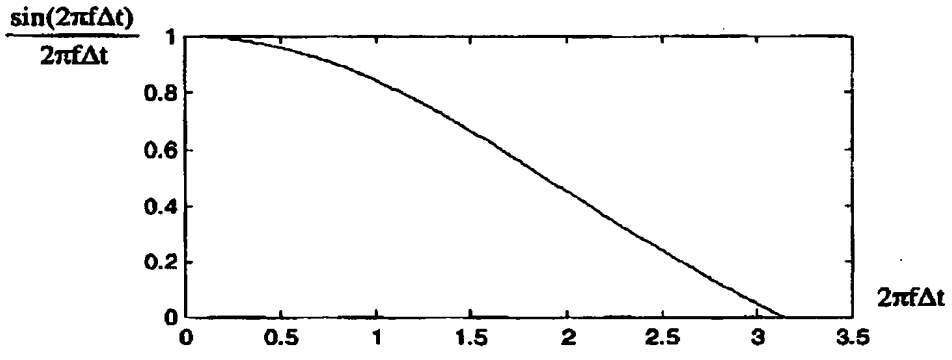


FIG. 1C

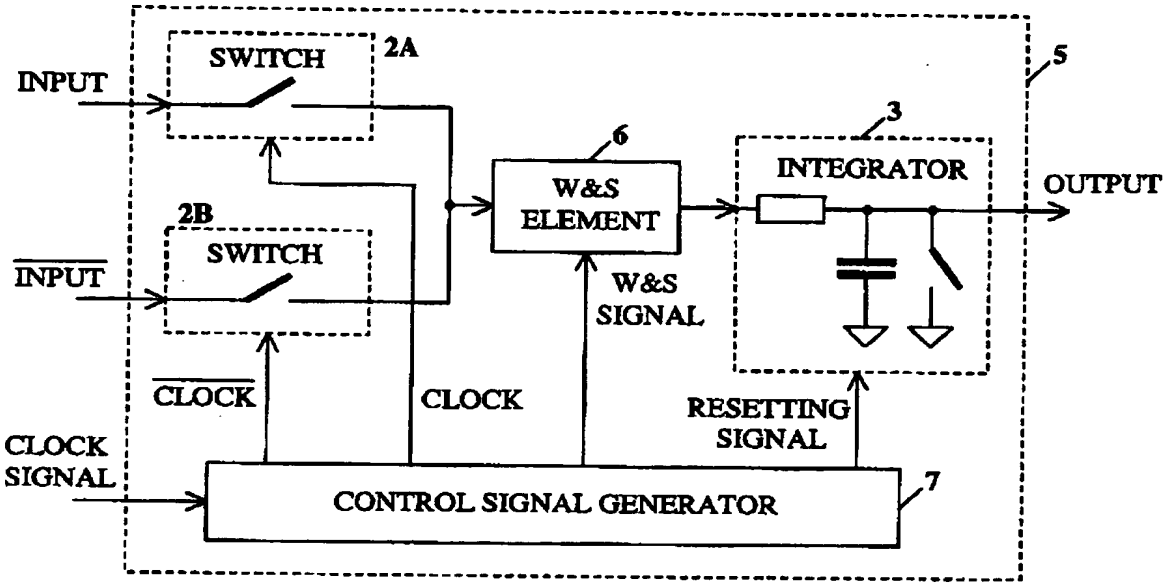

SWITCH
2A
INPUT
5
3
6
INTEGRATOR
W&S
ELEMENT
OUTPUT
2B
SWITCH
INPUT
W&S
SIGNAL
CLOCK
CLOCK
RESETTING
SIGNAL
CLOCK
SIGNAL
CONTROL SIGNAL GENERATOR
7

FIG. 2A

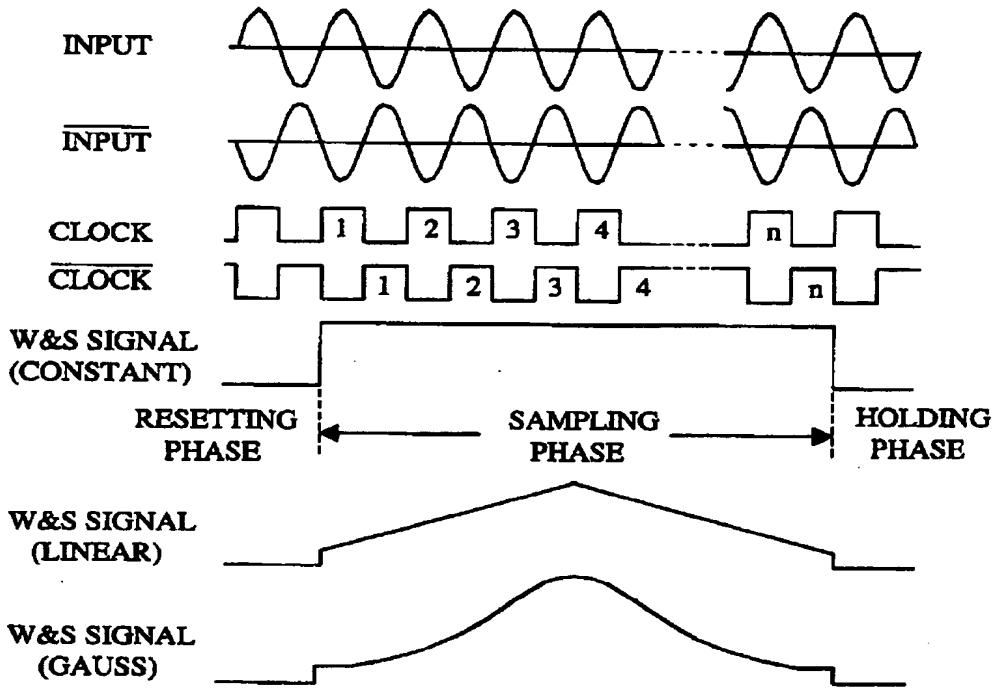

INPUT
INPUT
CLOCK
1
2
3
4
n
CLOCK
1
2
3
4
n
W&S SIGNAL
(CONSTANT)
RESETTING
PHASE
SAMPLING
PHASE
HOLDING
PHASE
W&S SIGNAL
(LINEAR)
W&S SIGNAL
(GAUSS)

FIG. 2B

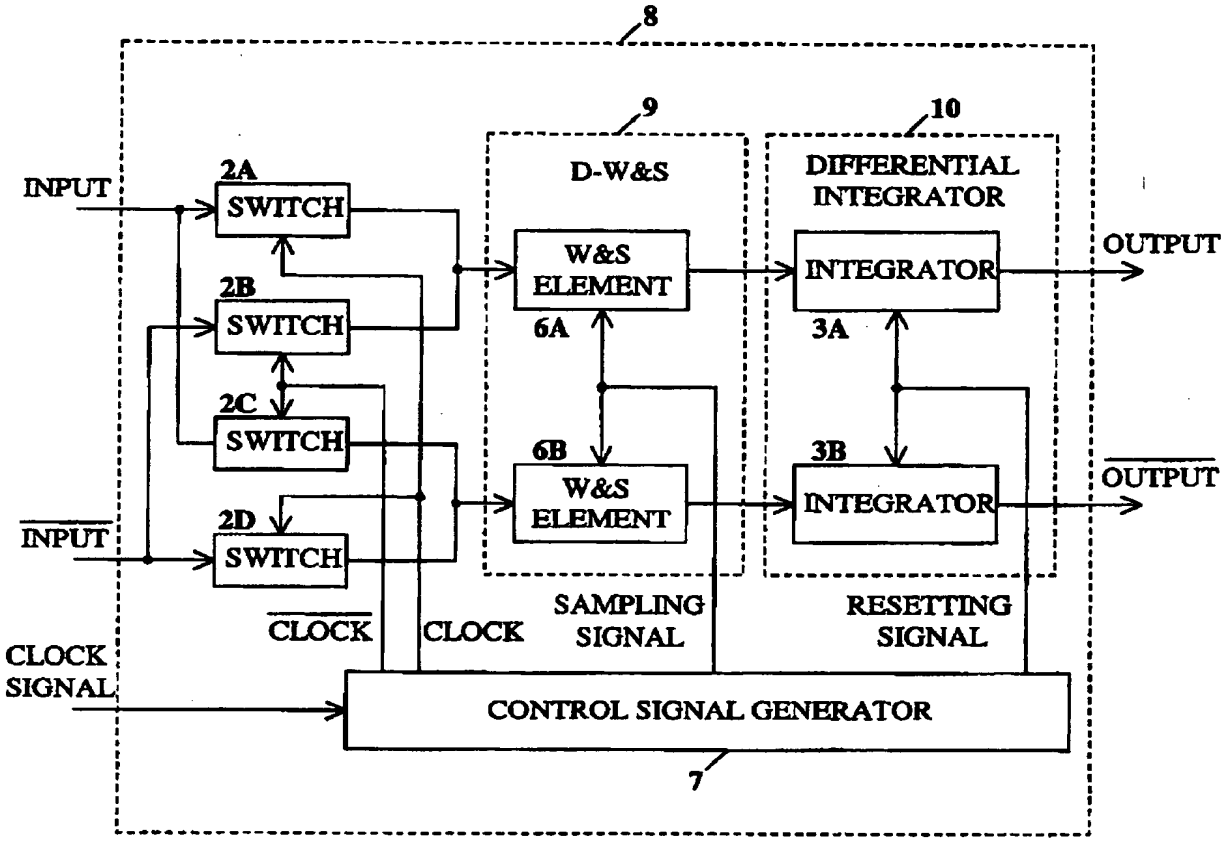

8
9
10
D-W&S
DIFFERENTIAL INTEGRATOR
INPUT
2A
SWITCH
2B
SWITCH
2C
SWITCH
2D
SWITCH
INPUT
W&S ELEMENT
6A
6B
W&S ELEMENT
INTEGRATOR
3A
3B
INTEGRATOR
OUTPUT
OUTPUT
CLOCK
CLOCK
SAMPLING SIGNAL
RESETTING SIGNAL
CLOCK SIGNAL
CONTROL SIGNAL GENERATOR
7

FIG. 3

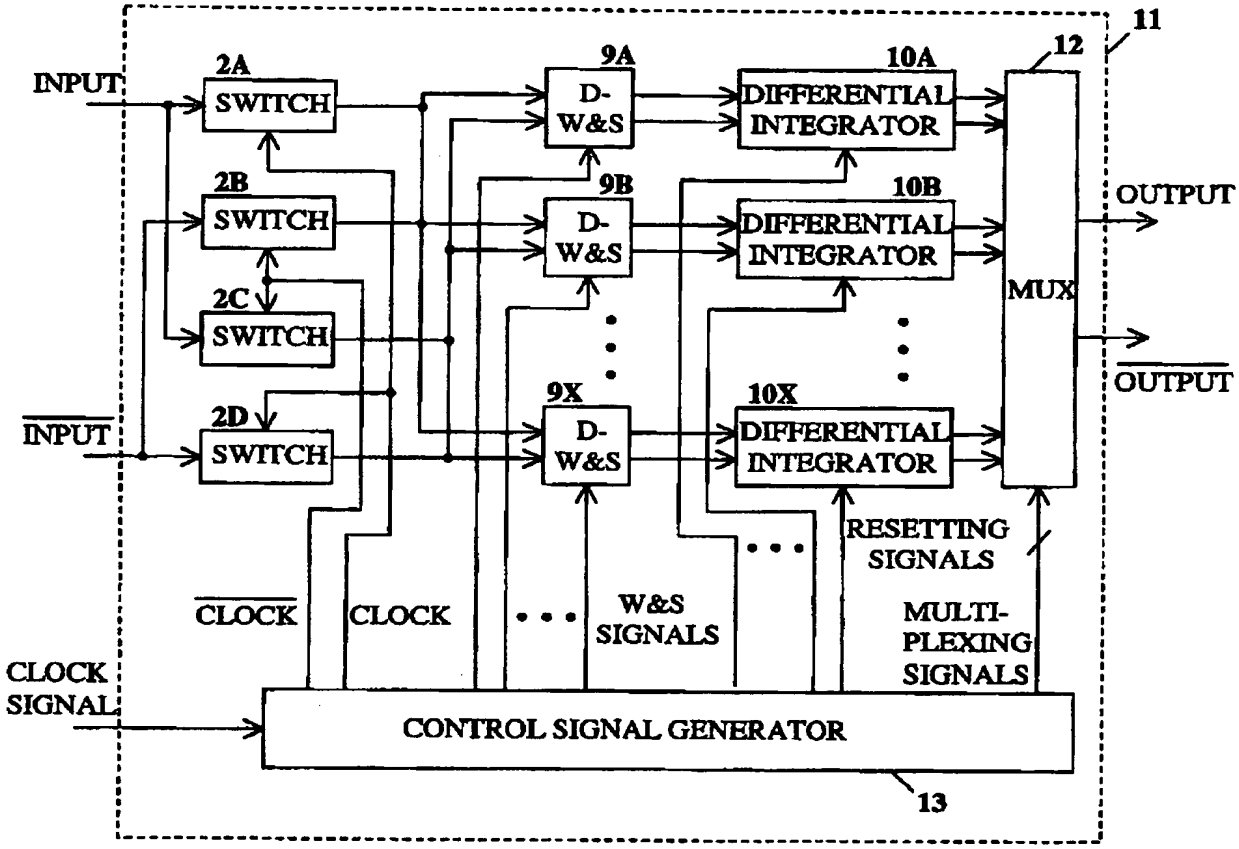

11
12
INPUT
2A
SWITCH
9A
D-
W&S
10A
DIFFERENTIAL
INTEGRATOR
2B
SWITCH
9B
D-
W&S
10B
DIFFERENTIAL
INTEGRATOR
OUTPUT
2C
SWITCH
MUX
INPUT
2D
SWITCH
9X
D-
W&S
10X
DIFFERENTIAL
INTEGRATOR
OUTPUT
RESETTING
SIGNALS
CLOCK
CLOCK
W&S
SIGNALS
MULTI-
PLEXING
SIGNALS
CLOCK
SIGNAL
CONTROL SIGNAL GENERATOR
13

FIG. 4

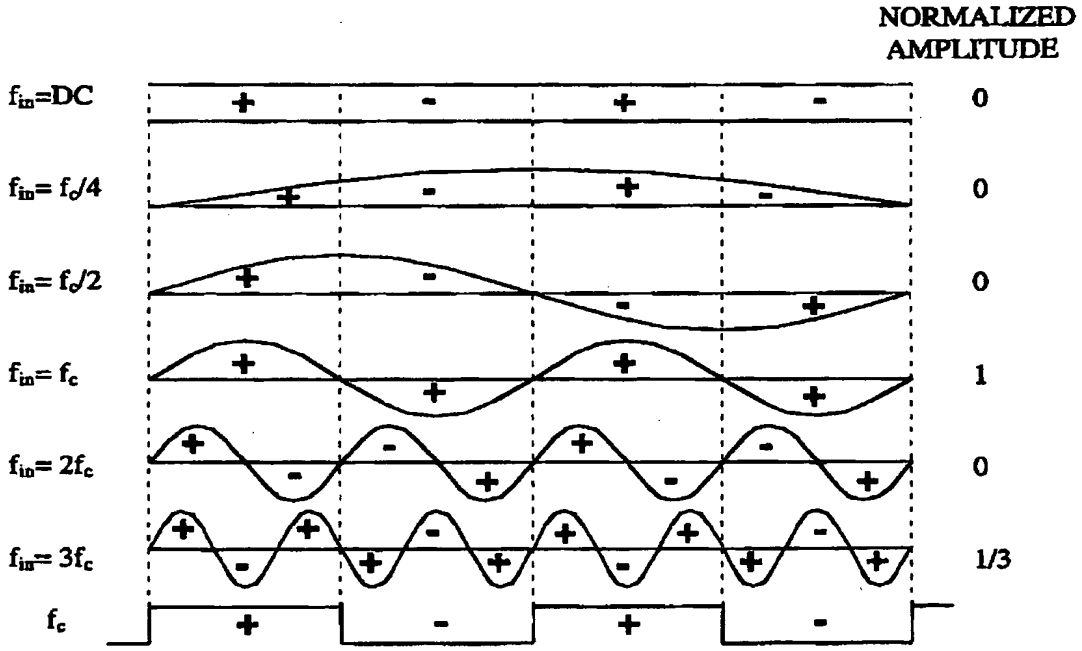

NORMALIZED AMPLITUDE
f_{in}=DC
f_{in}= f_c/4
f_{in}= f_c/2
f_{in}= f_c
f_{in}= 2f_c
f_{in}= 3f_c
f_c
0
0
0
1
0
1/3

FIG. 5

NORMALIZED AMPLITUDE

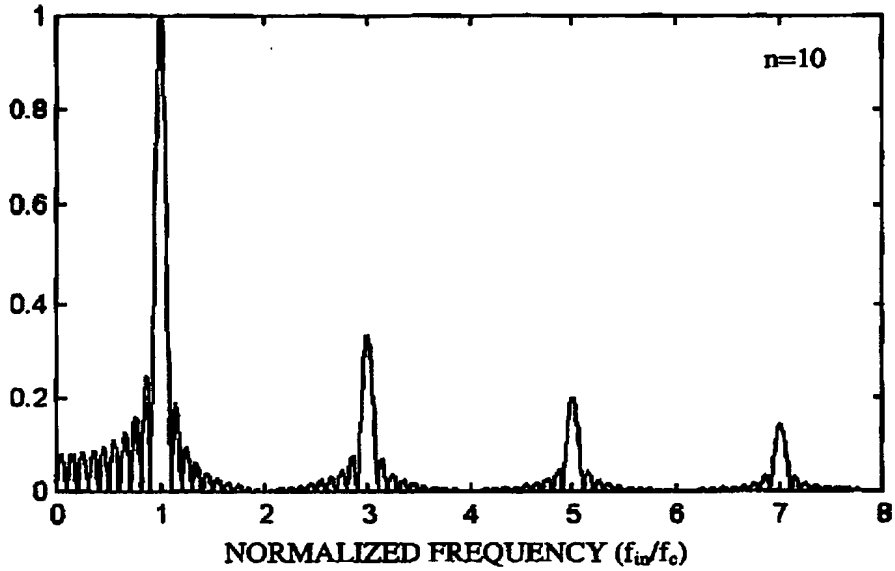
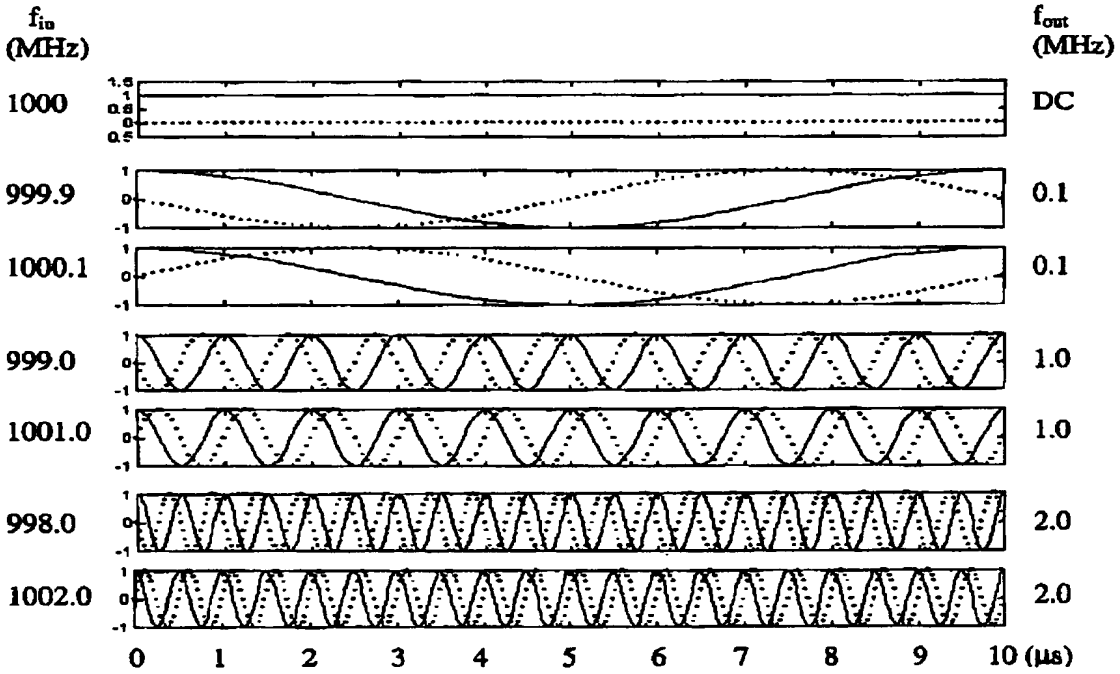


FIG. 6A



Note: 1. f_c=1000 MHz.
2. I in solid line and Q in dash line.

FIG. 6B

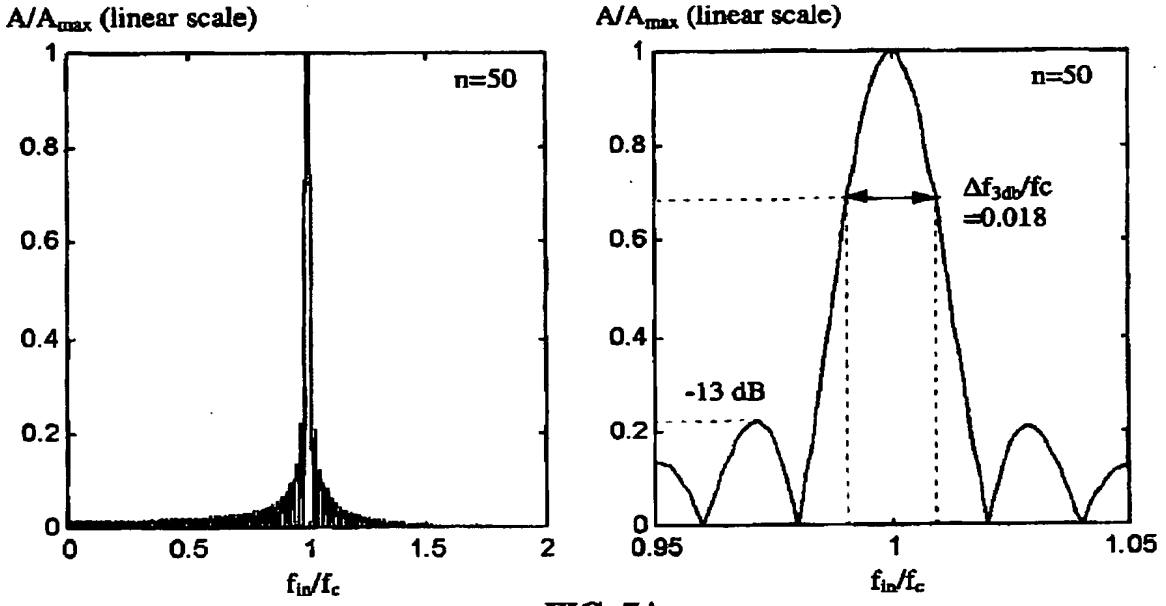

A/A_max (linear scale)
n=50
f_in/f_c
A/A_max (linear scale)
n=50
Δf_3db/fc
=0.018
-13 dB
f_in/f_c

FIG. 7A

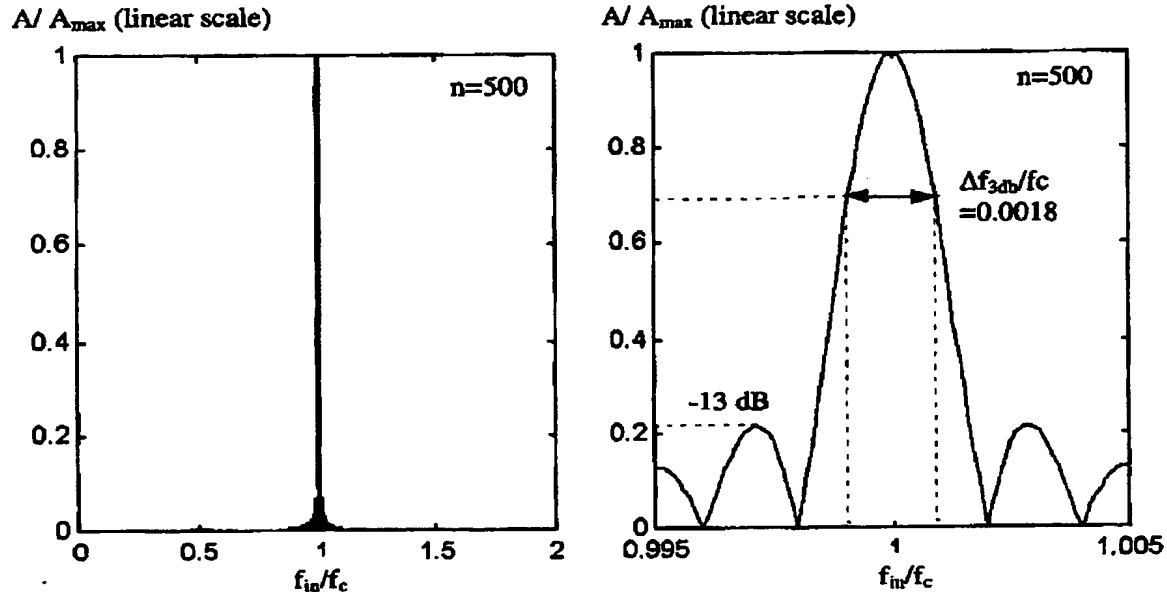

A/ A_max (linear scale)
n=500
f_in/f_c
A/ A_max (linear scale)
n=500
Δf_3db/fc
=0.0018
-13 dB
f_in/f_c

FIG. 7B

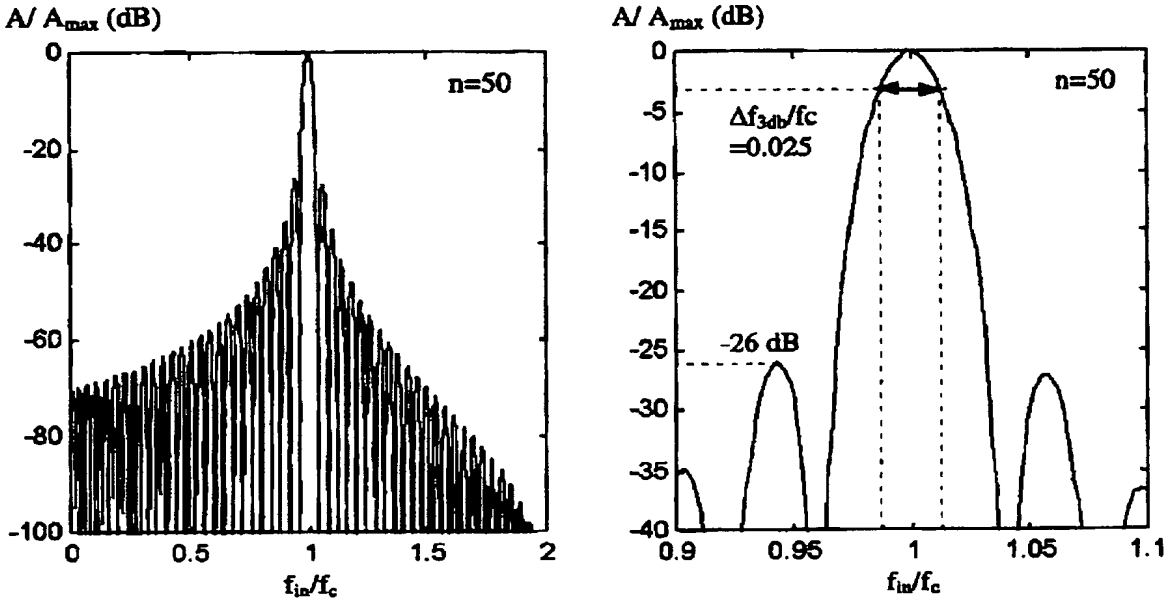

A/ Amax (dB)
n=50
fin/fc
A/ Amax (dB)
n=50
Δf3db/fc
=0.025
-26 dB
fin/fc

FIG. 8A

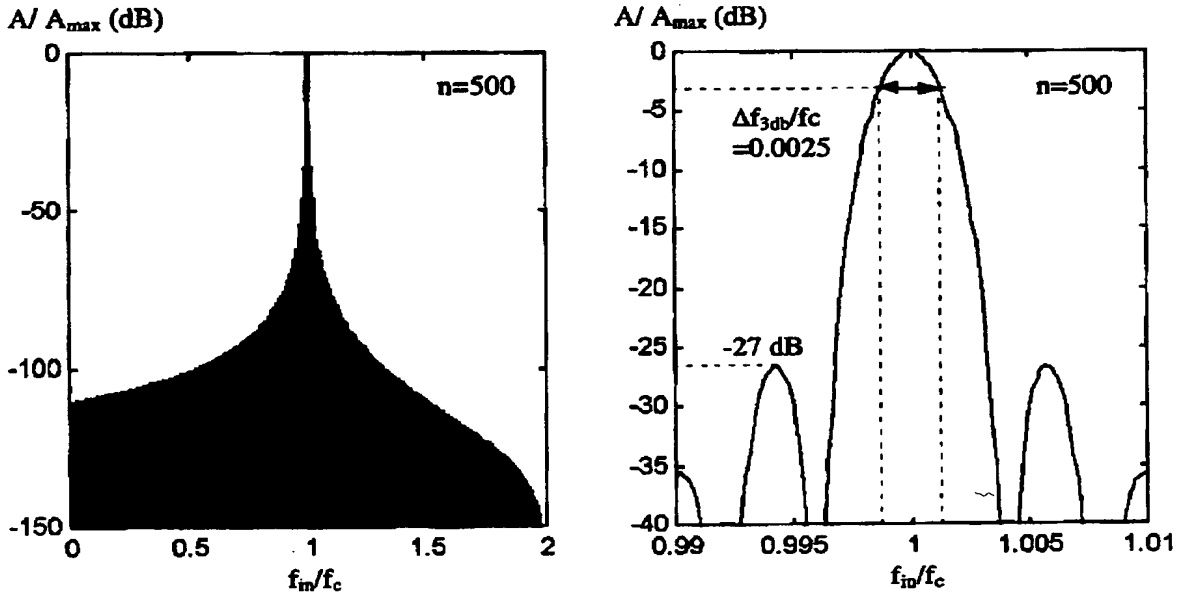

A/ Amax (dB)
n=500
fin/fc
A/ Amax (dB)
n=500
Δf3db/fc
=0.0025
-27 dB
fin/fc

FIG. 8B

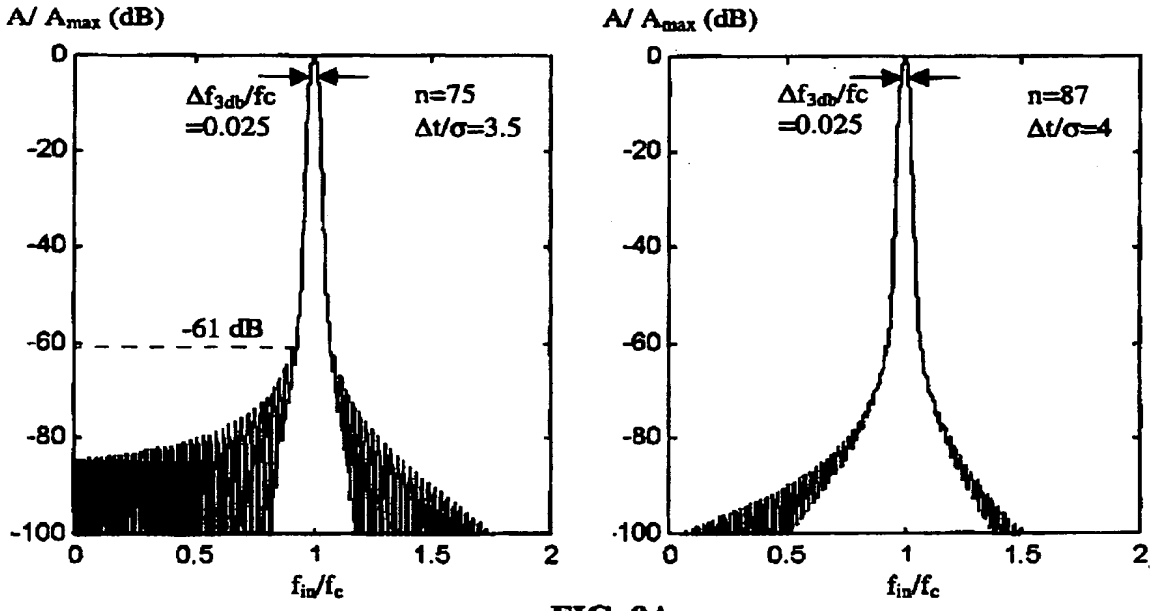

A/ Amax (dB)
Δf3db/fc =0.025
n=75
Δt/σ=3.5
-61 dB
fin/fc
A/ Amax (dB)
Δf3db/fc =0.025
n=87
Δt/σ=4
fin/fc

FIG. 9A

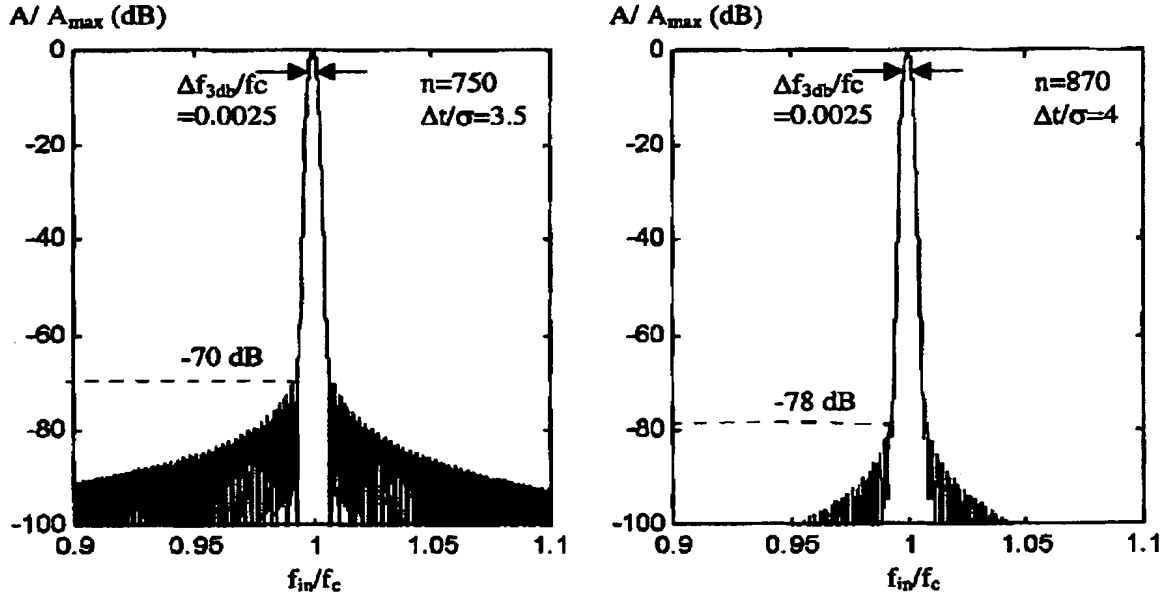

A/ Amax (dB)
Δf3db/fc =0.0025
n=750
Δt/σ=3.5
-70 dB
fin/fc
A/ Amax (dB)
Δf3db/fc =0.0025
n=870
Δt/σ=4
-78 dB
fin/fc

FIG. 9B

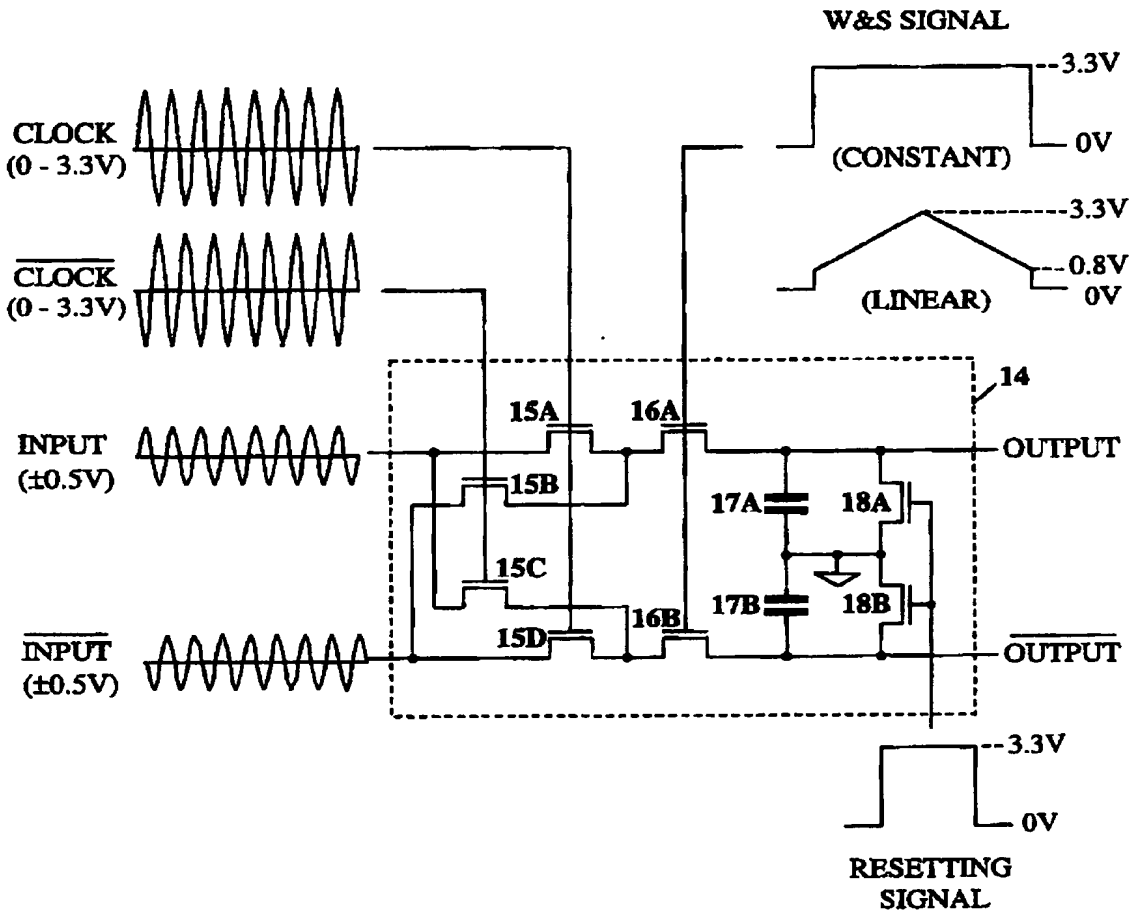

W&S SIGNAL
3.3V
0V
(CONSTANT)
3.3V
0.8V
0V
(LINEAR)
CLOCK
(0 - 3.3V)
CLOCK
(0 - 3.3V)
INPUT
(±0.5V)
INPUT
(±0.5V)
14
15A
16A
15B
15C
15D
16B
17A
17B
18A
18B
OUTPUT
OUTPUT
3.3V
0V
RESETTING
SIGNAL

FIG. 10

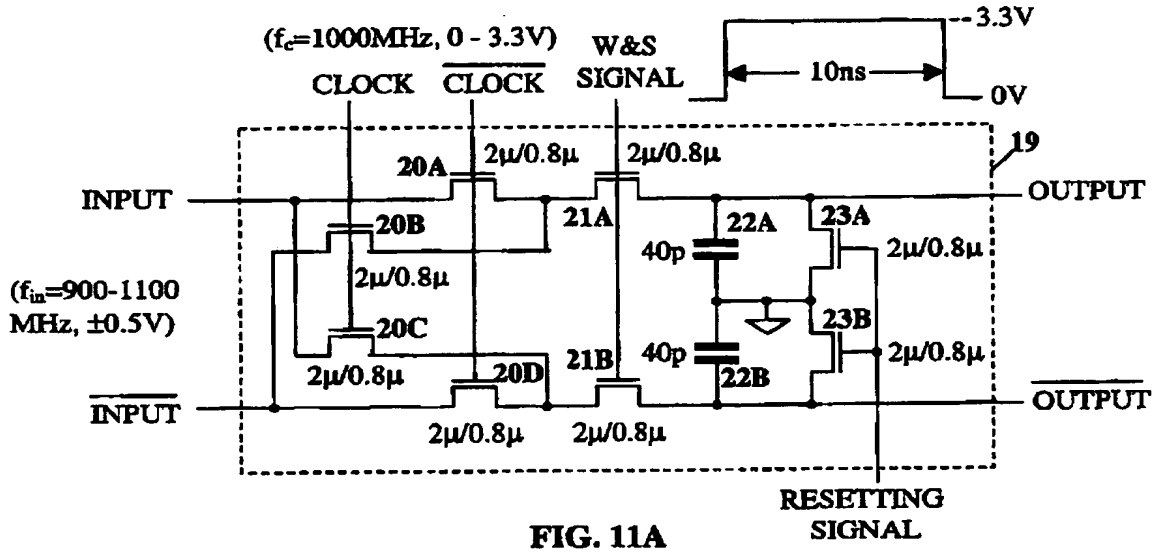
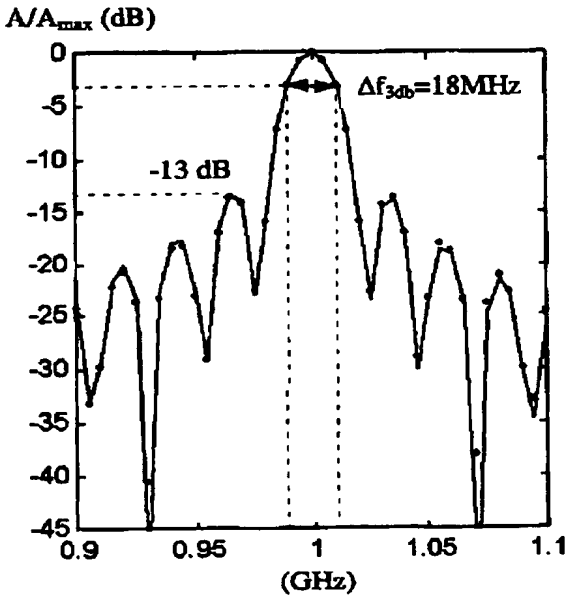


FIG. 11A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 11B

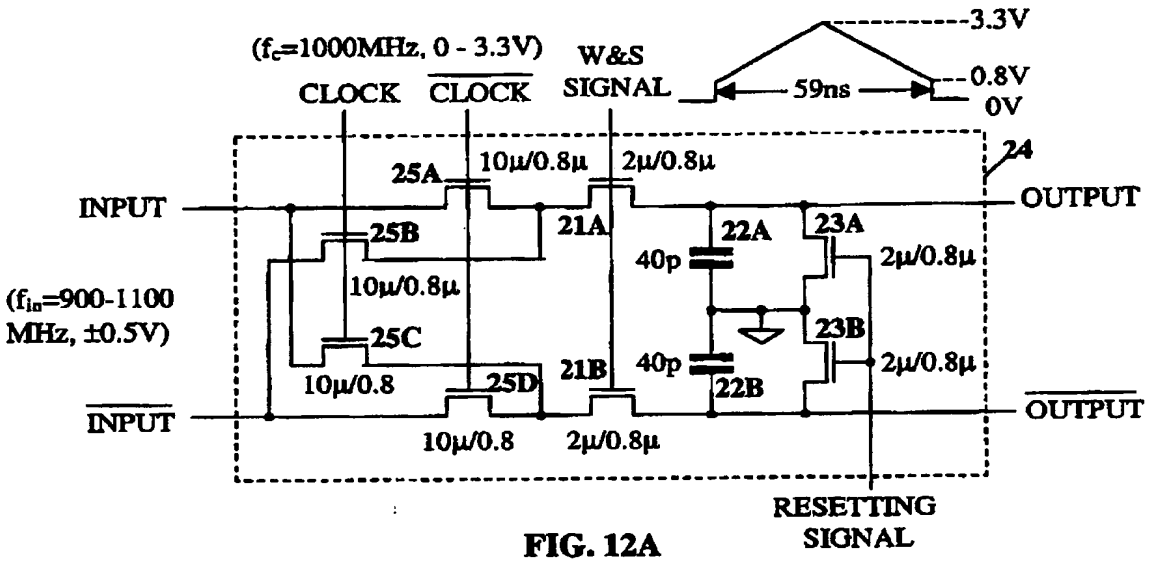
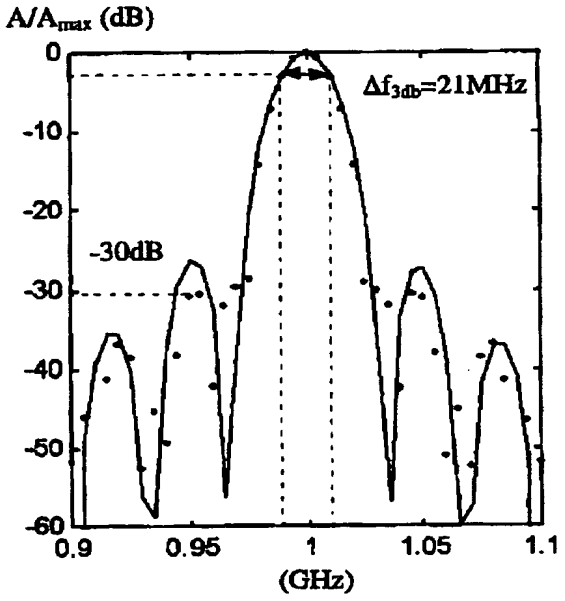


FIG. 12A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 12B

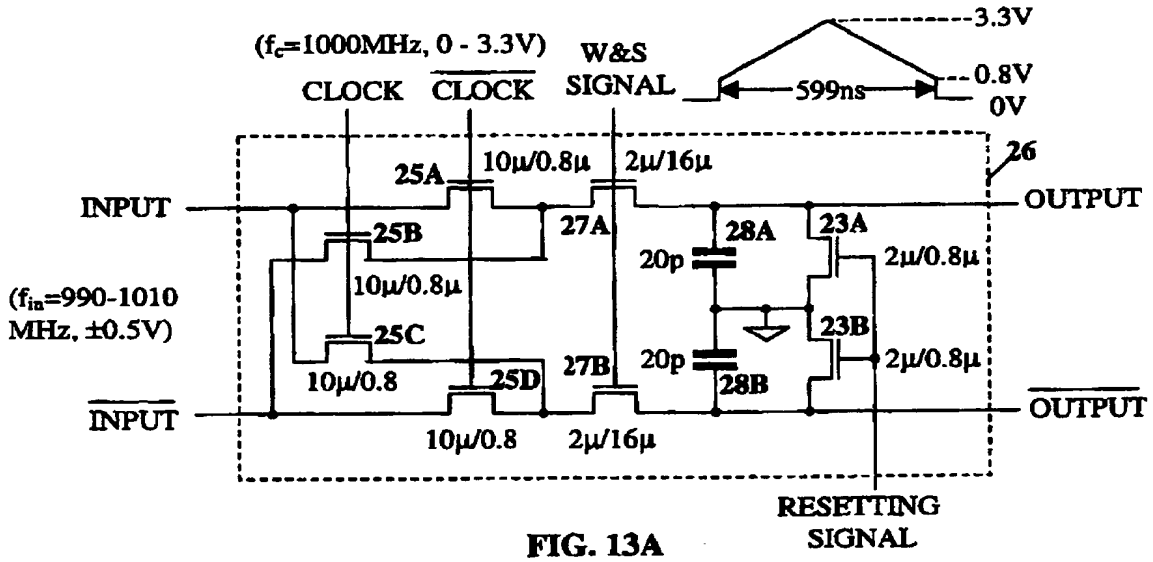
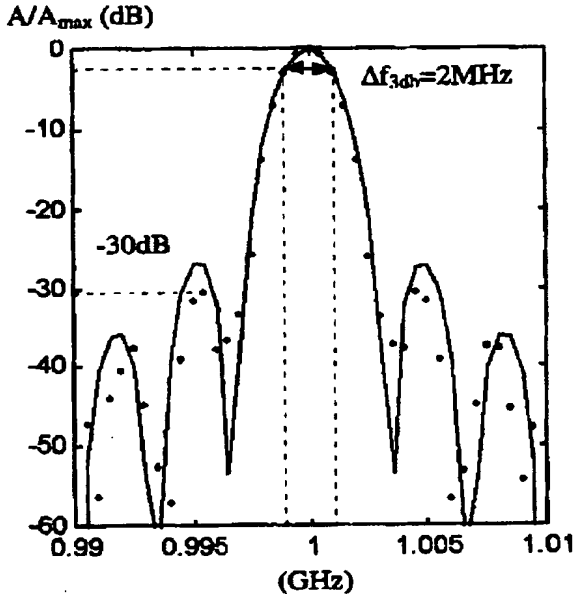


FIG. 13A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 13B

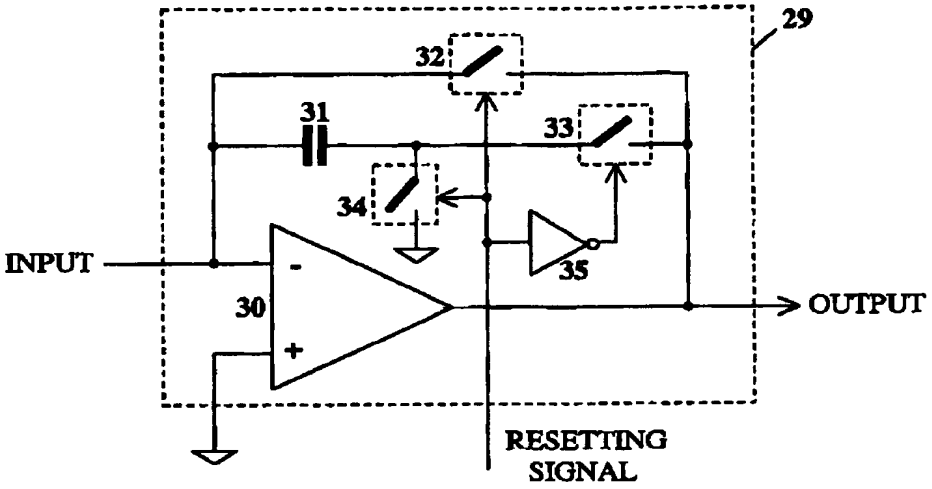


FIG. 14A

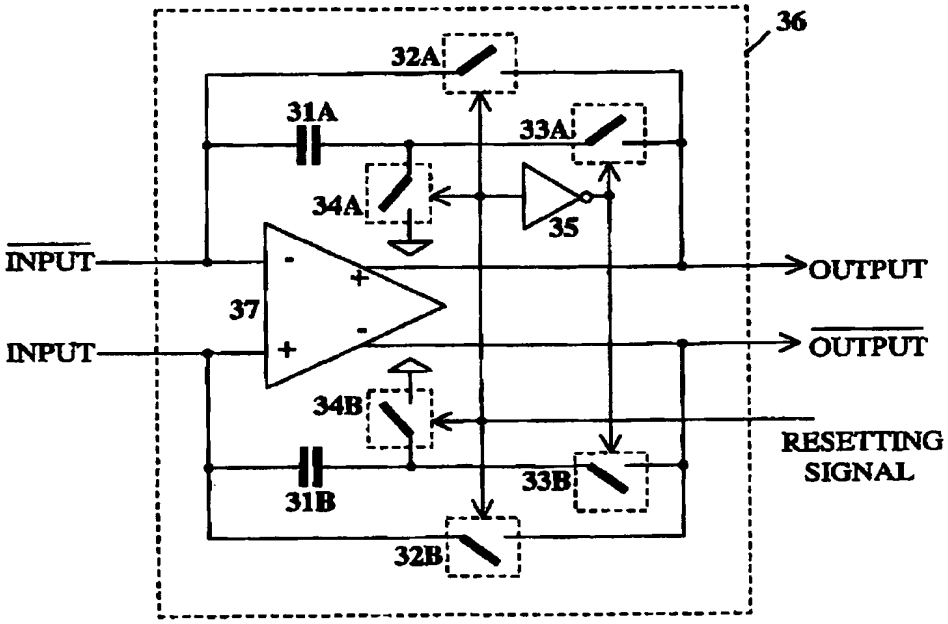


FIG. 14B

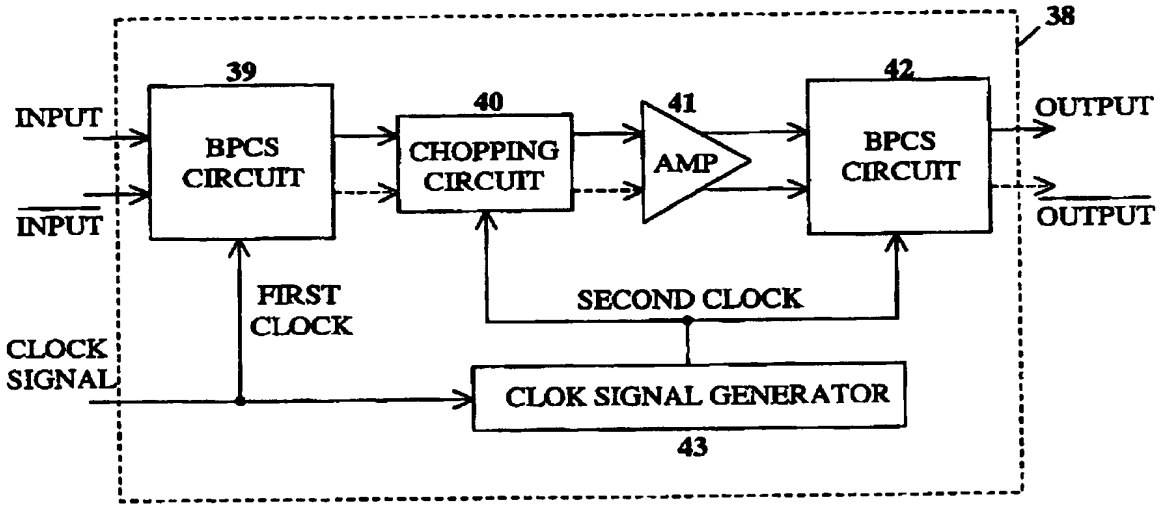

38
39
40
41
42
INPUT
INPUT
BPCS CIRCUIT
CHOPPING CIRCUIT
AMP
BPCS CIRCUIT
OUTPUT
OUTPUT
FIRST CLOCK
SECOND CLOCK
CLOCK SIGNAL
CLOK SIGNAL GENERATOR
43

FIG. 15

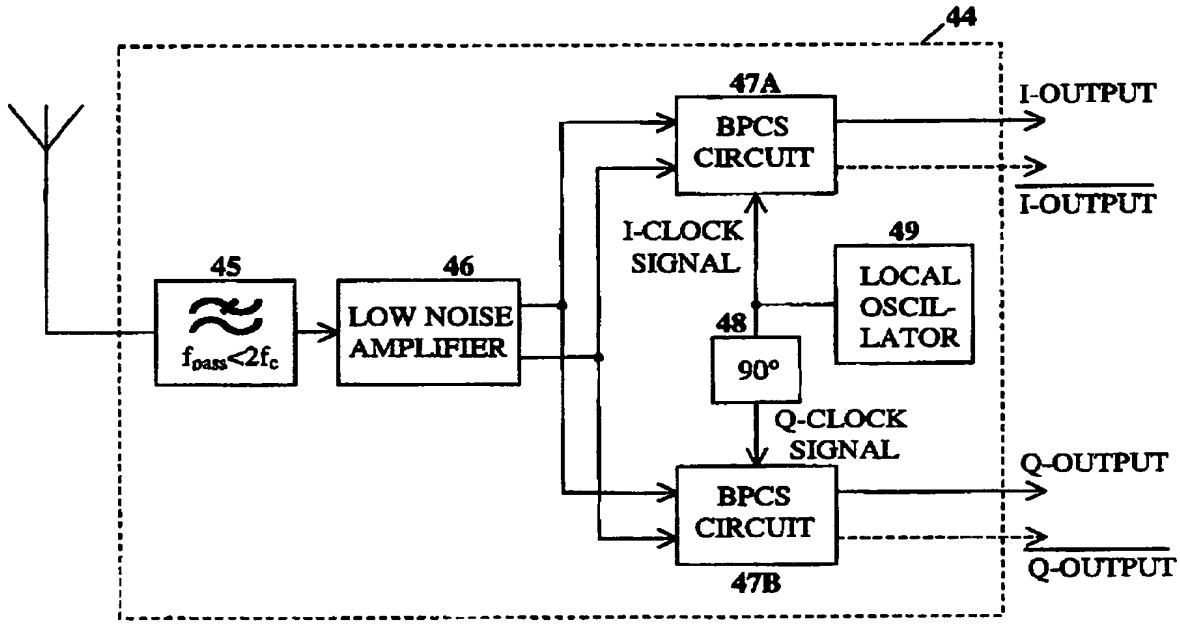

44
47A
BPCS CIRCUIT
I-OUTPUT
I-OUTPUT
I-CLOCK SIGNAL
49
LOCAL OSCIL-LATOR
45
46
LOW NOISE AMPLIFIER
$f_{pass}<2f_c$
48
90°
Q-CLOCK SIGNAL
Q-OUTPUT
BPCS CIRCUIT
Q-OUTPUT
47B

FIG. 16